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(54) Electronic component package using cap wafer and method therefore

(57) A component (10) includes a substrate (15), a cap wafer (23), and a protection layer (28) formed over a surface of the cap wafer (23). Together, the protection layer (28) and the cap wafer (23) form a cap structure (39) that is bonded to the substrate (15) via a bonding layer (33). An opening (47) is formed in the cap wafer (23) by etching the cap wafer (23). The protection layer (28) provides protection during etching of the cap wafer (23) for the underlying bonding layer (33) and devices (11,12) formed in the substrate (15).

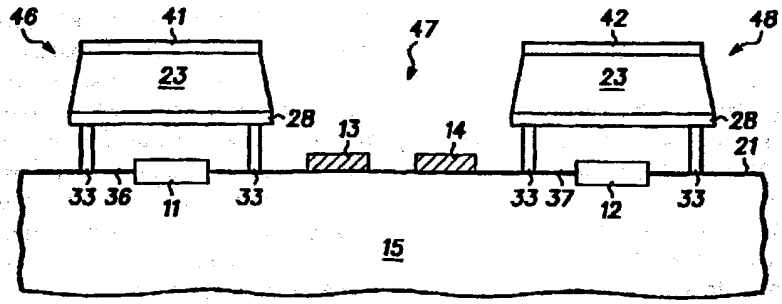

FIG. 3

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Description

Field of the Invention

[0001] The present invention relates, in general, to electronic components and, more particularly, to protection of electronic devices using cap wafers.

Background of the Invention

[0002] Due to their size, devices such as microelectronic sensors and integrated circuits are vulnerable to damage from handling, small particles, and moisture. Micromachined devices are typically placed in an enclosure to protect them during operation. One prior art component includes a cap wafer bonded to a semiconductor substrate for enclosing and hermetically sealing an electronic sensor from the environment. Holes are formed in the cap wafer prior to bonding the cap wafer to the substrate. Holes in the cap wafer provide for electrically connecting the sensor to external circuitry.

[0003] The holes in the cap wafer may weaken the mechanical structural reliability of the cap wafer. One solution to this problem is to increase the thickness of the cap wafer so that the structural integrity of the cap wafer is improved. However, increasing the thickness of the cap wafer also increases the size and cost of the microelectronic device.

[0004] Accordingly, it would be advantageous to have a component that provides protection to micromachined devices therein during operation. It would be of further advantage for the component to be size and cost efficient. In addition, it would be advantageous to have a method for manufacturing the component that is compatible with standard semiconductor processes.

Brief Description of the Drawings

[0005]

FIG. 1 is a cross-sectional view of a portion of a component during processing in accordance with an embodiment of the present invention;

FIG. 2 is a cross-sectional view of the component of FIG. 1 at a later stage of processing; and

FIG. 3 is a cross-sectional view of the component of FIG. 2 at an even later stage of processing.

Detailed Description of the Drawings

[0006] FIG. 1 is a cross-sectional view of a portion of a component 10 during processing in accordance with the present invention. In this embodiment, component 10 is a semiconductor component that includes devices 11 and 12 formed in a substrate 15. Component 10 further includes conductive traces 13 and 14 formed on a surface 21 of substrate 15. Substrate 15 comprises a semiconductor material such as, for example, silicon. Devices 11 and 12 can be integrated circuits or micromachined transducers such as pressure sensors or accelerometers. Although devices 11 and 12 are shown formed in substrate 15, this is not a limitation of the present invention. Devices 11 and 12 can also be formed on surface 21 of substrate 15.

[0007] Conductive traces 13 and 14 are formed by disposing a layer of electrically conductive material on surface 21 and patterning this conductive material using photolithographic and etch techniques. For example, conductive traces 13 and 14 may be formed by coating the electrically conductive material with a layer of photoresist (not shown), exposing the portions of the electrically conductive material to be removed (using, for example, photolithographic techniques), and etching the exposed portions of the electrically conductive material. Suitable conductive materials for conductive traces 13 and 14 include copper, aluminum, copper alloys, aluminum alloys, or the like.

[0008] Component 10 includes a cap wafer 23 having a top surface 26 and a bottom surface 27. Cap wafer 23 comprises a semiconductor material such as, for example, silicon. Other suitable materials for cap wafer 23 include glass, quartz, polymer, or metal. A suitable range of thicknesses for cap wafer 23 is between approximately 50 microns and approximately 600 microns.

[0009] A protection layer 28 is disposed or grown on bottom surface 27 of cap wafer 23. Protection layer 28 has a top surface 30 and a bottom surface 31, wherein top surface 30 of protection layer 28 contacts bottom surface 27 of cap wafer 23. Preferably, protection layer 28 has a thickness ranging from approximately 0.2 microns to approximately 2 microns. Together, cap wafer 23 and protection layer 28 form a cap structure 39. Suitable materials for protection layer 28 include oxide or nitride.

[0010] Etch masks 41 and 42 are disposed on top surface 26 of cap wafer 23. Masks 41 and 42 are formed by disposing a layer of metal such as, for example, aluminum on top surface 26 of cap wafer 23 and pattering this metal layer using photolithographic and etch techniques. In addition to serving as masks during a subsequent etching step, masks 41 and 42 also provide electrical shielding for devices 11 and 12. Masks 41 and 42 are also referred to as masking layers and are preferably positioned over devices 11 and 12, respectively.

[0011] Cap structure 39 is bonded to substrate 15 using a layer of bonding material 33 to form cavities 36 and 37. By way of example, bonding material 33 is frit glass that is disposed on a portion of bottom surface 31 of layer 28 by screen printing. The frit glass, which is also referred to as a powder glass, is a mixture of glass particles dispersed in an organic binder or solvent. After screen printing, the frit glass is heated to volatilize the organic binder or solvent. Cap structure 39 containing the frit glass is then placed in contact with surface 21 of substrate 15. Heat is applied and the frit glass then

enamels or flows to bond cap structure 39 to substrate 15 and provide cavities 36 and 37. After cap structure 39 is bonded to substrate 15, devices 11 and 12 are hermetically sealed within cavities 36 and 37, respectively. Bonding material 33, a portion of protection layer 28, and a portion of substrate 15 form walls of the hermetically sealed cavities 36 and 37. Although bonding material 33 is described as frit glass, this is not a limitation of the present invention. Bonding material 33 can also comprise gold, metal, or alkali glass. Further, other types of bonding processes can be employed to bond cap structure 39 to substrate 15. For example, anodic, eutectic, or thermocompression bonding can be employed for bonding cap structure 39 to substrate 15.

[0012] It should be noted that although the embodiment discussed herein is a semiconductor device, this is not a limitation of the present invention. The present invention can be applied to other applications such as applications using biosensors, wherein the biosensors are protected using a cap material. In these other applications, substrate 15 can be comprised of other materials such as glass, quartz, metal, etc. Preferably, cap wafer 23 and substrate 15 are formed of materials having substantially the same coefficients of thermal expansion.

[0013] FIG. 2 is a cross-sectional view of component 10 at a later stage of processing. It should be understood that the same reference numerals are used in the figures to denote the same elements. FIG. 2 shows component 10 after removal of portions of cap wafer 23.

[0014] A wet etch solution comprising an etchant such as, for example, tetramethylammonium hydroxide (TMAH) is utilized to etch cap wafer 23. Portions of cap wafer 23 not covered by masks 41 and 42 are removed during etching. The wet etch solution does not affect protection layer 28, which functions as an etch stop. In the embodiment shown in FIG. 2, bonding layer 33 is frit glass which can be damaged by a wet etch solution comprising TMAH. Protection layer 28 serves as an etch stop layer for protecting bonding layer 33 during etching of cap wafer 23. Preferably, protection layer 28 comprises a material that is resistant to a wet etch solution comprising TMAH. Suitable materials for protection layer 28 include oxide or nitride.

[0015] FIG. 3 is a cross-sectional view of component 10 at an even later stage of processing. FIG. 3 shows component 10 after removal of portions of protection layer 28.

[0016] Openings 46, 47, and 48 can also be formed using a dry etch process such as a Reactive Ion Etch (RIE) or a Deep Reactive Ion Etch (DRIE) with either a chlorine or fluorine based chemistry. The portions of protection layer 28 underlying masks 41 and 42 are not removed during the dry etch process. The diameter of opening 47 can range between approximately 500 microns and 2000 microns. Opening 47 provides for electrical connection to conductive traces 13 and 14. For example, bond wires (not shown) may be coupled to conductive traces 13 and 14 through opening 47. Although not shown, conductive traces 13 and 14 can be used to electrically couple devices 11 and 12 to other portions of component 10.

[0017] As discussed hereinbefore, protection layer 28 is disposed on bottom surface 27 of cap wafer 23 to provide protection for bonding layer 33, which can be damaged during a chemical wet etch. Alternatively, component 10 can be formed without protection layer 28 and openings 46, 47, and 48 can be formed using a single etching step. For example, if protection layer 28 is omitted, then cap wafer 23 can be etched using a single etching step that includes using either an appropriate wet etch or dry etch process. When protection layer 28 is not included in component 10, bonding layer 33 is disposed on a portion of bottom surface 27 of cap wafer 23 and cap wafer 23 is bonded to substrate 15 via bonding layer 33. Cavities 36 and 37 are formed by cap wafer 23, bonding layer 33, and substrate 15.

[0018] It should be noted that cavities 36 and 37 are not necessary in all cases. For example, bonding layer 33 can surround and contact devices 11 and 12.

[0019] Because openings 46, 47, and 48 are formed after cap structure 39 and substrate 15 are bonded together, cap wafer 23 can be a relatively thin wafer, thereby decreasing the overall stack thickness of component 10. For example, cap wafer 23, which is comprised of silicon, can have a thickness of less than approximately 50 microns. Prior art silicon cap wafers typically have thicknesses of greater than 375 microns. Further, forming openings 46, 47, and 48 after cap wafer 23 is bonded to substrate 15 simplifies the layout and manufacturing of component 10.

[0020] By now it should be appreciated that a component and method for manufacturing the component is provided. The present invention provides a component that provides for protection of its elements during operation. The method of the present invention is compatible with standard semiconductor processes including CMOS processes. Further, the method reduces the number of processing steps for manufacturing a component having a cap wafer.

Claims

1. A component (10), comprising:

   a substrate (15) having a device (11) thereon;
   a bonding layer (33) disposed on a portion of a surface of the substrate;
   a cap wafer (23) over the substrate; and
   a protection layer (28) having a first surface (30) and a second surface (31), wherein the first surface of the protection layer contacts a first surface of the cap wafer and the second surface of the protection layer is bonded to the surface of the substrate via the bonding layer

and wherein the protection layer, the bonding layer, and the substrate form a cavity that encloses the device.

2. The component of claim 1, further including a conductive layer (13) formed on the surface of the substrate and wherein the cap wafer has an opening (47) formed over the conductive layer after the bonding layer is disposed on the protection layer.

3. The component of claim 1, further including a masking layer (41) formed on a portion of a second surface of the cap wafer that is over the device.

4. The component of claim 1, wherein the bonding layer (33) comprises frit glass.

5. A method for manufacturing a component, comprising the steps of:

providing a cap wafer (23);
disposing a protection layer (28) over a first surface (30) of the cap wafer, wherein a first surface of the protection layer is bonded to the first surface of the cap wafer;
disposing a bonding layer (33) over a portion of a second surface (31) of the protection layer;
bonding the second surface of the protection layer to a surface of a substrate via the bonding layer; and
forming an opening (47) in the cap wafer after the step of disposing the bonding layer.

6. The method of claim 5, wherein a micromachined device (11) in the substrate is enclosed within a cavity formed by the bonding layer (33), the protection layer (28), and the substrate (15).

7. The method of claim 5, wherein the step of forming the opening (47) includes etching the cap wafer (23) using a wet etch solution, wherein the protection layer (28) is formed of a material that is resistant to the wet etch solution so that the protection layer serves as an etch stop layer for protecting the bonding layer (33) during etching of the cap wafer.

8. The method of claim 7, further including the step of disposing a masking layer (41) over a portion of a second surface of the cap wafer, wherein portions of the cap wafer not covered by the masking layer are removed during etching of the cap wafer.

9. The method of claim 5, wherein the bonding layer (33) comprises frit glass, the cap wafer (23) comprises silicon, the substrate (15) comprises silicon, and the protection layer (28) comprises oxide or nitride.

10. The method of claim 5, further including the step of disposing a conductive layer (13) over the surface of the substrate, wherein the opening (47) provides for electrical connection to the conductive layer.

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 12 2968

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Y	US 5 323 051 A (ADAMS VICTOR J ET AL) 21 June 1994 (1994-06-21) * the whole document *	1-10	H01L23/04 H01L23/10
Y	EP 0 855 748 A (NIPPON TELEGRAPH & TELEPHONE) 29 July 1998 (1998-07-29) * column 7, line 26 - line 43; figures 1,2 *	1-10	
A	PATENT ABSTRACTS OF JAPAN vol. 1996, no. 05, 31 May 1996 (1996-05-31) -& JP 08 022941 A (TOPPAN PRINTING CO LTD), 23 January 1996 (1996-01-23) * abstract *	1-10	
A	PATENT ABSTRACTS OF JAPAN vol. 1998, no. 02, 30 January 1998 (1998-01-30) -& JP 09 260745 A (NISSAN MOTOR CO LTD), 3 October 1997 (1997-10-03) * abstract *	1-10	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01L
A	US 5 061 987 A (HSIA YUKUN) 29 October 1991 (1991-10-29) * column 4, line 26 - line 39; figures 1,2 *	1-10	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	2 February 2001	Munnix, S

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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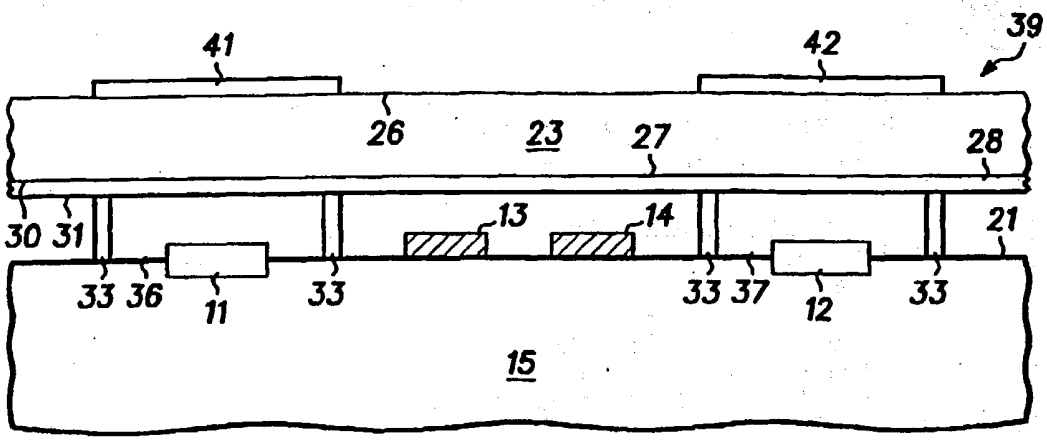
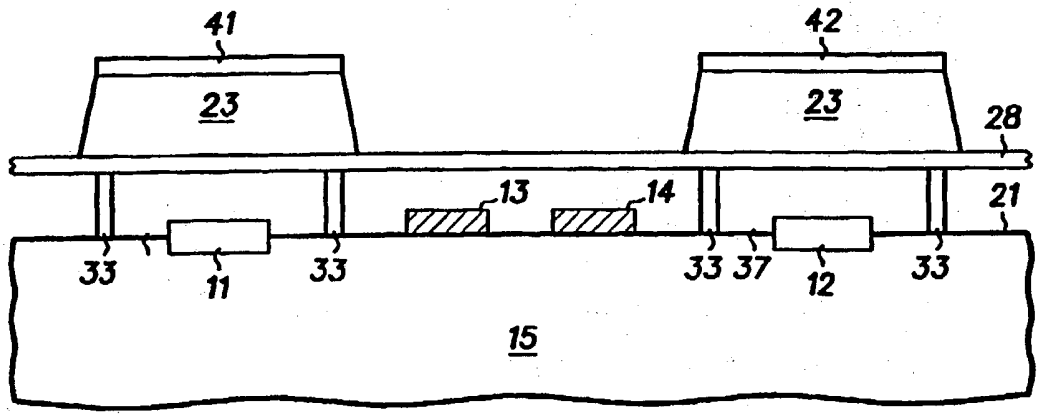
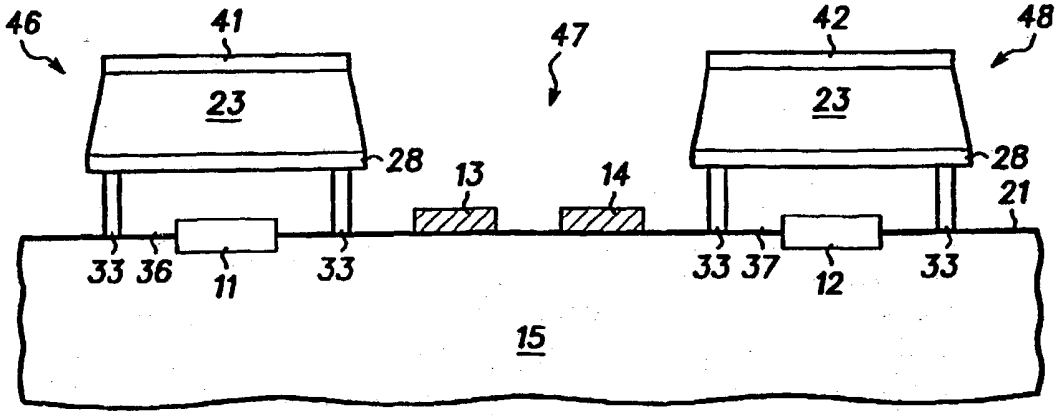


10 FIG. 1



10 FIG. 2



10 FIG. 3

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 12 2968

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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